What is claimed is:

[Claim 1] 1. A method for accessing memory, comprising the steps of:

dividing a memory into N memory blocks;

receiving a plurality of line data, and sequentially writing the line data into N memory blocks, wherein N is an integer; and

after writing more than N/2+1 memory blocks, starting to read the line data stored in the memory blocks.

[Claim 2] 2. The method for accessing memory of claim 1, wherein the memory is a single port memory.

[Claim 3] 3. The method for accessing memory of claim 2, wherein the reading step is started after the writing of the N/2+2 memory blocks is completed.

[Claim 4] 4. The method for accessing memory of claim 2, wherein the reading step is started from the memory blocks which are written in a sequence of the 1^{st} memory block and the $(N/2+1)^{th}$ memory block.

[Claim 5] 5. The method for accessing memory of claim 1, wherein the storage capacity of the memory is the same as the size of the line data.

[Claim 6] 6. The method for accessing memory of claim 5, wherein the memory is a single port memory.

[Claim 7] 7. The method for accessing memory of claim 6, wherein the reading step is started after the writing of the N/2+2 memory blocks is completed.

[Claim 8] 8. The method for accessing memory of claim 6, wherein N is a positive even number greater than 7.

[Claim 9] 9. The method for accessing memory of claim 6, wherein the reading step is started from the memory blocks which are

written in a sequence of the 1st memory block and the (N/2+1)th memory block.

[Claim 10] 10. The method for accessing memory of claim 1, wherein the writing further comprises the steps of:

dividing the line data into a plurality of even data and a plurality of odd data according to a sequence of the line data; and

writing the even data and odd data into the N memory blocks, respectively, wherein the memory block for writing the even data is different from the memory block for writing the odd data.

[Claim 11] 11. The method for accessing memory of claim 10, wherein the storage capacity of the memory is the same as the size of the line data.

[Claim 12] 12. The method for accessing memory of claim 10, wherein the memory is a single port memory.

[Claim 13] 13. The method for accessing memory of claim 10, wherein the reading step is started after the writing of the N/2+2 memory blocks is completed.

[Claim 14] 14. The method for accessing memory of claim 10, wherein N is a positive even number greater than 7.

[Claim 15] 15. The method for accessing memory of claim 10, wherein the reading step is started from the memory blocks which are written in a sequence of the 1st memory block and the (N/2+1)th memory block.

[Claim 16] 16. The method for accessing memory of claim 11, wherein the reading step is started after the writing of the N/2+2 memory blocks is completed.

[Claim 17] 17. The method for accessing memory of claim 11, wherein the memory is a single port memory.

[Claim 18] 18. An apparatus performing the method of claim 1.

[Claim 19] 19.The apparatus of claim 18, wherein the memory is a single port memory.